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FLIP-CHIP PACKAGE

FIELD OF THE INVENTION

The present invention is generally relating to a flip-chip package, particularly to a flip-chip package comprising a chip carrier consisted of a dummy die and a substrate with an opening.

BACKGROUND OF THE INVENTION

In a conventional flip-chip package, a IC chip with a plurality of bumps is directly flip-chip mounted on a substrate, such as a printed circuit board or ceramic circuit board. A conventional flip-chip package had been brought up from R.O.C. (Republic Of China, Taiwan) Patent No. 457664 entitled “directly-downset flip-chip semiconductor package and its manufacturing process”. A chip is flip-chip mounted onto a substrate with a chip-cavity. The chip cavity of the substrate forms a plurality of dimple bonding pads for bonding the bumps of the chip. Due to the different thermal expansion coefficient between the chip and the substrate, the flip-chip mounting region (i.e. bumps) of the chip bears considerable thermal stress so that a warpage or bump-breaking easily takes place on the substrate.

In order to solve the problem of warpage on the substrate caused by thermal stress, a flip chip package had been disclosed in R.O.C. Patent No. 489,496 that a filling compound with a larger coefficient of thermal expansion (CTE) than that of the substrate is coated around the flip-chip region of the substrate for lessening substrate warpage of flip-chip package. But the chip is still directly flip-chip mounted on the substrate, such as ceramic or printed circuit board. The stress still exists at the chip. Flip-chip pads formed on the substrate are critical to match the fine pitch bumps of flip chip, and also the entire flip chip package has a thicker thickness.

SUMMARY

A primary object of the present invention is to provide a flip-chip package with a

1 dummy die. The dummy die without any electrically calculating function is mounted to
2 a substrate having an opening to constitute a chip carrier with a chip cavity. The
3 dummy die has a surface with a redistribution layer (RDL) for electrically connecting a
4 flip-chip mounting type chip and the substrate so as to achieve fine pitch flip-chip
5 mounting, thinner flip chip package and eliminating stress at the flip-chip mounting type
6 chip.

7 A second object of the present invention is to provide a flip-chip package. The
8 flip-chip package comprises a chip carrier which consists of a dummy die and a substrate
9 with opening. The dummy die without any electrically calculating function but has a
10 surface possessing a redistribution layer for flip-chip mounting a chip. A chip cavity of
11 the chip carrier is formed by the surface of the dummy die and the opening of the
12 substrate, and the dummy die becomes an electrical interface medium between a chip
13 mounted on the dummy chip and the substrate, so that the failure of directly flip-chip
14 mounting die to substrate will be abated. Fine pitch flip-chip mounting, thinner flip-chip
15 package and high heat dissipation are able to be achieved.

16 A third object of the present invention is to provide a chip carrier for flip-chip
17 package. The chip carrier consists of a substrate with opening and a dummy die with a
18 redistribution layer. A surface of the dummy die with the redistribution layer is attached
19 on the opening of the substrate to form a chip cavity of the chip carrier for flip-chip
20 connection of a chip.

21 In accordance with the flip-chip package of the present invention, the flip-chip
22 package comprises a substrate, a dummy die, at least a chip and a packaging body. The
23 substrate has a top surface, a bottom surface and an opening passing through the top and
24 bottom surface, such as printed circuit board, which has an unmatched coefficient of
25 thermal expansion (larger) with that of the chip. The dummy die has a surface with a
26 redistribution layer electrically connected to the substrate. It is preferable that the
27 surface of the dummy die is bonded on the bottom surface of the substrate corresponding

1 to the opening. The dummy die and the substrate are assembled to form a composite
2 chip carrier with a chip cavity. The chip is flip-chip mounted on the surface of the
3 dummy die inside the chip cavity and electrically connected to the substrate through the
4 redistribution layer of the dummy die. The packaging body is formed in the opening of
5 the substrate.

6 DESCRIPTION OF THE DRAWINGS

7 Fig.1 is a cross-sectional view illustrating a flip-chip package in accordance with a
8 first embodiment of the present invention.

9 Fig.2 is a top view illustrating a dummy die of a flip-chip package in accordance
10 with the first embodiment of the present invention.

11 Fig.3 is a cross-sectional view illustrating stacked multiple flip-chip packages in
12 accordance with the first embodiment of the present invention.

13 Fig.4 is a cross-sectional view illustrating a flip-chip package in accordance with a
14 second embodiment of the present invention.

15 DETAILED DESCRIPTION OF THE PRESENT INVENTION

16 According to the first embodiment shown in Fig.1, a flip-chip package 100
17 comprises a substrate 110, a chip 120, a dummy die 130 and a packaging body 140. The
18 substrate 110 can be a printed circuit board made from BT resin, FR-4 resin or FR-5 resin.
19 The substrate 110 possesses a top surface 111, a bottom surface 112 and an opening 113
20 passing through the top surface 111 and the bottom surface 112. It is preferable that the
21 substrate 110 is a build-up multi-layer printed circuit board so as to have a stair 114
22 around the opening 113.

23 The dummy die 130 is disposed on the bottom surface 112 of the substrate 110
24 corresponding to the opening 113. In this embodiment, the dummy die 130 which
25 thickness is about 200 μm (micro meter) has a surface 131 with a redistribution layer 133
26 (RDL) and a corresponding exposed surface 132. The surface 131 of the dummy die
27 130 is attached onto the bottom surface 112 of the substrate 110 by means of an adhesive

1 tape 115 in order to form a composite chip carrier with a chip cavity. The chip cavity is
2 formed by the surface 131 of the dummy die 130 and the opening 113 of the substrate
3 110 for accommodating the chip 120. The dummy die 130 is a silicon substrate without
4 any electrically calculating function or is a substrate with the same or similar CTE as the
5 chip 120. The redistribution layer 133 is formed by an integrated circuit manufacturing
6 process. As shown in Fig.1 and Fig.2, the redistribution layer 133 includes a plurality of
7 flip-chip pads 134 for flip-chip connection of the chip 120 and a plurality of connecting
8 pads 135 arraying around the surface 131 of the dummy die 130. Each of the flip-chip
9 pads 134 and corresponding connecting pads 135 are connected by an integrated circuit
10 trace 136. The pitch of the flip-chip pads 132 is smaller than that of the connecting
11 pads 135. Since the redistribution layer 133 may be manufactured by utilizing
12 sputtering and photolithography of integrated circuit manufacturing technique. Firstly a
13 metal layer is formed on the surface 131 of the dummy die 130 by means of sputtering,
14 then the flip-chip pads 134, the connecting pads 135 and the integrated circuit 136 are
15 formed after forming photoresist, exposing, developing and etching. It is better to add a
16 passivation layer (not shown in the drawing) on the surface 131 of the dummy die 130 for
17 coating the integrated circuit traces 136 and exposing the flip-chip pads 134 and the
18 connecting pads 135. Therefore, the pitch of the flip-chip pads 134 may not be larger
19 than 150 μm , even may reach 70~90 μm or more closely. Furthermore, the connecting
20 pads 135 on the dummy die 130 are electrically connected with the substrate 110 (pads
21 on the stair 114) by electrically connecting elements, such as bonding wires 137 or TAB
22 leads so that wire-bonding height is lowered to thin the entire package thickness.

23 The chip 120 is a IC chip with electrically calculating function, such as
24 microprocessor, microcontroller, memory or ASIC. The chip 120 is flip-chip mounted
25 onto the substrate 131 of the dummy die 130 inside the chip cavity (opening 113). The
26 chip 120 has an active surface forming a plurality of bumps 121, and the chip 120 is
27 smaller than the dummy die 130 in size. By means of flip-chip mounting (or called C4)

1 technique, the bumps 121 of the chip 120 are bonded to the flip-chip pads 132 of the
2 redistribution layer 131. Both the dummy die 130 and the chip 120 have the similar
3 coefficient of thermal expansion so that the bumps 121 of the chip 120 won't be
4 influenced by the thermal stress for eliminating the flip-chip stress of the chip 120.

5 Besides, the packaging body 140 is formed in the opening 113 of the substrate 110
6 to protect the chip 120 by dispensing or molding. In this embodiment, the packaging
7 body 140 can be formed as thin as possible by dispensing liquid compound into the
8 opening 113. Furthermore, the flip-chip package further comprises a plurality of solder
9 balls 150 planted on the bottom surface 112 of the substrate 110, or the top surface 111 of
10 the substrate 110 according to another different design of the substrate 110. The
11 flip-chip pads 134 of the dummy die 130 made by the integrated circuit manufacturing
12 process can match the bumps 121 high density arranged on the chip 120. The dummy
13 die 130 is used to become an electrical interface medium between the chip 120 and the
14 substrate 110 for avoiding the failure of directly flip-chip mounting the chip 120 to the
15 substrate 110 and reaching fine pitch of flip-chip mounting. By means of assembling
16 the dummy die 130 and the substrate 110 to a chip carrier, the flip-chip package 100 is
17 able to be thinned substantially.

18 Moreover, as shown in Fig.3, in another embodiment the substrate 110 has a
19 plurality of connection pads 116 on the upper surface 111. The connection pads 116 are
20 electrically connected with the solder ball 150 by internal multi-layer wiring design of the
21 substrate 110. Thus a plurality of flip-chip packages 100 can be stacked vertically by
22 connecting the solder ball 150 of an upper flip-chip packages 100 with the connection
23 pads 116 of an lower flip-chip packages 100. Thus the connection pads 116 of the
24 substrate 110 are provided for connecting outer terminals of a stack semiconductor
25 package in supper thin configuration.

26 In the second embodiment of the present invention, another flip-chip package 200 is
27 illustrated in Fig.4. The flip-chip package 200 comprises a semiconductor chip 220 and

1 a composite chip carrier composed of a substrate 210 and a dummy die 230. The
2 substrate 210 is a printed circuit board. The substrate 210 has a top surface 211, a
3 bottom surface 212 and an opening 213 passing through the top surface 211 and the
4 bottom surface 212. The dummy die 230 has a top surface with a redistribution layer
5 231 formed by the integrated circuit manufacturing process and a corresponding exposed
6 bottom surface. A plurality of bumps 232 are formed on the top surface of the dummy
7 die 230 and electrically connect the redistribution layer 231 for electrically connecting
8 the substrate 210. A chip cavity of the chip carrier is formed by the top substrate of the
9 dummy die 230 and the opening 213 of the substrate 210. The bottom surface of the
10 dummy die 230 has a high thermal-conducting metal layer 233, such as gold or copper.
11 The thermal-conducting metal layer 233 is formed by sputtering method for enhancing
12 heat dissipation. At least a semiconductor chip 220 with electrically calculating
13 function is flip-chip mounted onto the top surface of the dummy die 230 inside the chip
14 cavity (opening 213) so that the bumps 221 of the chip 220 are bonded onto the
15 redistribution layer 231 (i.e. flip-chip pads) and electrically connected to the printed
16 circuit board 210 passing through the peripheral connecting pads of redistribution layer
17 231 and the bumps 232. Therefore, in order to avoid directly flip-chip mounting the
18 chip 220 onto a printed circuit board, the dummy die 230 is used for flip-chip connection
19 of the chip 220 to reach eliminating flip-chip stress of the chip 220, fine pitch flip-chip
20 mounting and thinner flip-chip package. Besides, a packaging body 240 formed after
21 electrically connecting step by dispensing method, then a plurality of solder ball 250 are
22 planted to the bottom surface 212 of the substrate 210.

23 The above description of embodiments of this invention is intended to be illustrated
24 and not limiting. Other embodiments of this invention will be obvious to those skilled
25 in the art in view of the above disclosure.

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